HACETTEPE UNIVERSITY
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
ELE-314 ELECTRONICS LABORATORY III

EXPERIMENT 1
SWITCHING CIRCUITS WITH BJT AND JFET

1. PURPOSE:

To investigate the switching properties of BJT and JFET.

2. THEORY :

BJT : There exists three operating regions of BJT's namely; cut-off, saturation(SAT) and active. In digital applications transistor is operated in cut-off and sat. For this reason the input voltages driving the transistor into cut-off or sat have to be determined.

In order to determine whether the BJT is in cut-off or not, at first the terminals of the transistor is assumed to be open circuit and the voltage V_{BE} is determined. If the condition $V_{BE} < V_{BEon}$ (0.65 V for Si and 0.2 V for Ge transistors, but Ge transistors are no longer in use now) is satisfied, then the BJT is in cut-off.

To investigate the saturation condition, equivalent saturation circuit of BJT is used. In this case currents I_B and I_C are calculated separately.

If $\beta I_B > I_C$ then BJT is in SAT. If the transistor is neither in cut-off nor in saturation, then it is in active region and used as an amplifier. Circuit models of operation modes are shown in figure 1.

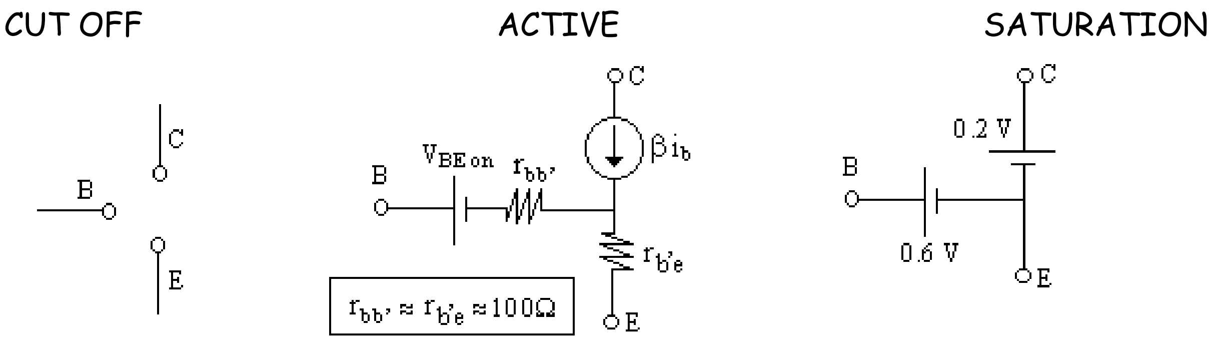

Figure 1: TRANSISTOR MODELS for BJT

JFET :

There exists three operating regions of JFET as shown in figure 2.

a) Cut off mode: $|V_{GS}| > |V_P|$ and $I_D = 0$ for any V_{DS}

b) Triode or ohmic region: $|V_{GS}| < |V_P|$ and $|V_{DS}| < |V_P| - |V_{GS}|$

c) Saturation region: $|V_{GS}| < |V_P|$ and $|V_{DS}| > |V_P| - |V_{GS}|$ where $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

The fundamental difference between BJT and JFET in a switching circuit is that the output voltage of the BJT in saturation can not be reduced below V_{CEsat} whilst the voltage V_{DS} of JFET can be reduced to zero, theoretically.

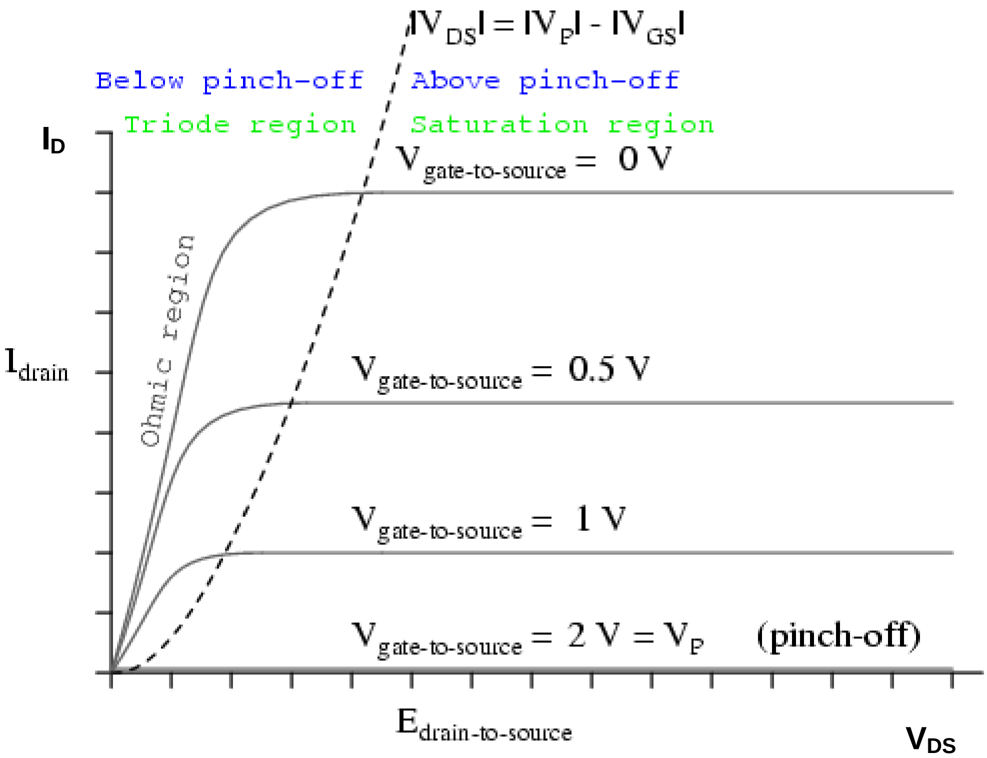

Figure 2: Characteristic curve of JFET

3. PRELIMINARY WORK :

3.1. Assuming the left hand side of the diode (including the diode) of the circuit is detached from the inverter to analyze as shown in figure 3.

a) Find the time constants showing the charge and discharge rates of the capacitor when the diode is ON or OFF (The forward resistance of the diode is 100Ω and the reverse resistance is 10 MΩ).

b) Sketch V_o for $V_S = \pm 5$ V and 1 KHz. square wave.

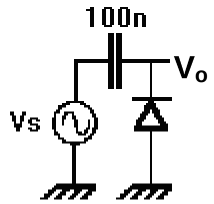

Figure 3: Input Circuit of the figure 2

3.2. For the circuit in figure 4, assume β≥125, V_{BEon} = 0.6 V, V_{BEon} = 0.8V, V_{CEsat} = 0.2 V, V_{cc}=12V. Choose the resistances among the component list given at the end of the preliminary work. Design the inverter circuit shown in figure 4 satisfying the following specifications.

a) Determine the inequality for R_1 which drives the transistor in saturation (V_s = ±5V, 1KHz square wave and the current through R_1 is less than or equal to 1 mA). Choose the closest standart value of R_1 from the component list at the end of experiment.

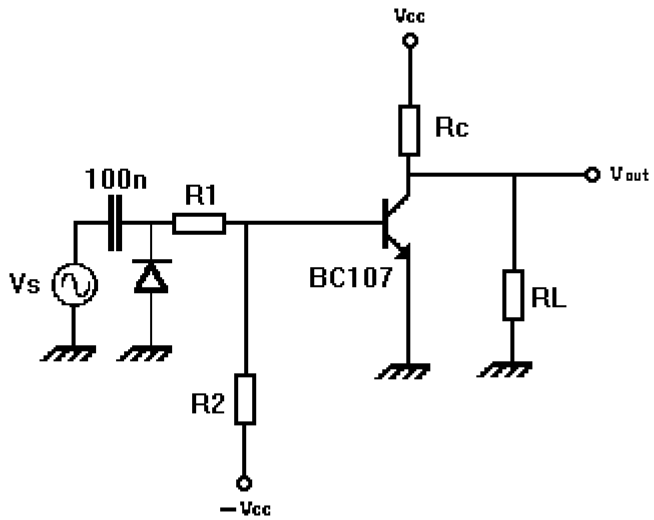

Figure 4. An BJT inverter circuit

b) If the load resistor $R_L \geq 5.6$ KΩ and $V_{out} \geq$ 10 V , then determine the inequality that should be satisfied by R_C . Choose the closest standart value from the component list.

c) With V_s = 0 and the transistor being in cut-off , determine the inequality of R_2 which makes the voltage $V_{BE} \leq$ -2 V.

d) Determine the inequality to be satisfied by R_2 to drive the transistor into saturation (V_s = ±5V, 1KHz square wave). Choose R_2 accordingly.

3.3. Draw the transfer characteristics of the inverter circuit you have designed for $R_L = \infty$.

3.4. Draw the transfer characteristics of the inverter circuit you have designed for R_L=5.6K.

3.5. Assume that I_{DSS}=0.2mA, V_p =-2.5V, V_{CC}=12 V. When V_{GS}=0V is applied to the circuit in figure 5, to fulfill saturation conditions what must be the minumum value of V_{DS} and corresponding resistance of potentiometer.

3.6. Draw the transfer characteristics of the JFET inverter circuit you have designed for $R_L = \infty$.

3.7. Draw the transfer characteristics of the JFET inverter circuit you have designed for R_L=5.6 KΩ.

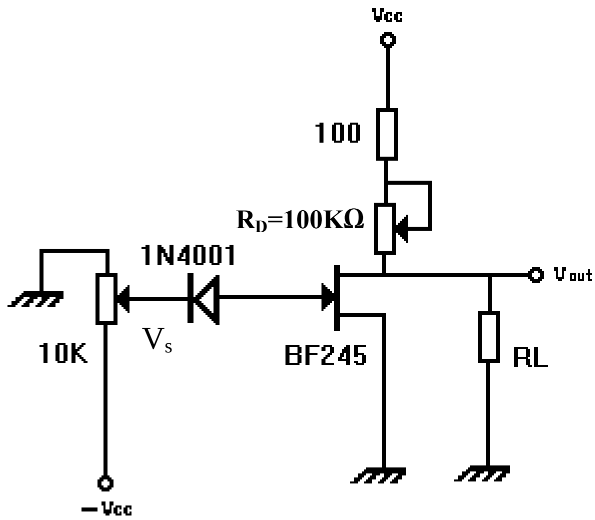

Figure 5: V_p =-2.5V, V_{CC}=12 V

3.8 Do the Pspice simulations of step 3.3, 3.4, 3.6 and 3.7

Resistors

100 Ω	#1
1K Ω	#1
5.6K Ω	#1
10 K Ω	#1
33 K Ω	#1
100KΩ - pot.	#1

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